

In re Patent Application of:  
**WRIGHT ET AL**  
Serial No. 10/040,153  
Filed: JANUARY 2, 2002

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IN THE SPECIFICATION:

Please replace paragraph [06] beginning at page 3, with the following rewritten paragraph:

[06] In the first embodiment, the counter is implemented as an up-counter and is initially preloaded by the receiver's micro-controller with a programmable value of zero. The contents of the counter are monitored by a logic circuit, which changes state and produces an output frame sync signal FS, upon the counter having counted up from its preloaded value up to a prescribed value (e.g., a value of  $N*8$ , where N is arbitrary and application dependent). The frame sync FS output of the logic circuit is monitored by the receiver's cell delineation mechanism for the purpose of controlling value to be preloaded into the counter, and thereby the number of clock signals to be counted by the counter in order [[the]] for the logic circuit to produce an output FS signal. In addition to being monitored by the cell delineation mechanism, the frame sync signal is fed back to reset or clear the contents of the counter to zero.

Please replace paragraph [26] beginning at page 9, with the following rewritten paragraph:

[26] Again, if cell delineation is not achieved ~~achieved~~ within a prescribed cell delineation acquisition window, the control processor 40 will again change the state of the control input 53 to the multiplexer 50 for the next succeeding frame sync count

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period. This repetitive selective modification of the start value of counter 30 effectively shifts the frame sync signal by one bit time earlier, on a periodic basis, causing the cell delineation mechanism to use the previous bit in time as a new start-of-octet location. Eventually, after some number of such one-bit shifts, cell delineation will be achieved, which terminates any additional preloading of the counter with a value other than zero.